For example, at paragraph 3 a definition of a media processor is given, and the definition is a system for processing audio, video, and graphics data.

At paragraph 153, it is disclosed that the embodiment described in the spec is for a media processor. I.e., a unit that processes graphics data.

At paragraphs 23-24, the specification references JPEG, MPEG, and DV, all graphics/video storage formats.

Many more examples exist within the specification.

Attached patents 6,473,087, 6,473,086, and 6,404,439 show that class 345/505 accept and originally classify similar parallel processor systems intended for processing graphics/video data.

Although the claims do not yet specifically claim the graphics/media aspect, the only direction which applicant has to move the claims should anticipating prior art be found is to add significant graphics processing to the claims. Therefore, case would be better examined in 345, as by the time prosecution is completed, the claims will be claiming graphics/media processing aspects.

US006473087B1

(12) **United States Patent**
Tsang

(10) **Patent No.: US 6,473,087 B1**
(45) **Date of Patent: Oct. 29, 2002**

(54) **METHOD AND SYSTEM FOR CONCURRENT PROCESSING OF SLICES OF A BITSTREAM IN A MULTIPROCESSOR (MP) SYSTEM**

(75) Inventor: **Ekman Tsang**, Vancouver (CA)

(73) Assignee: **Silicon Magic Corporation**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/464,327**

(22) Filed: **Dec. 15, 1999**

(51) **Int. Cl.**[7] **G06F 15/80**
(52) **U.S. Cl.** **345/505**; 345/504; 345/544; 345/555
(58) **Field of Search** 345/504, 505, 345/502, 544, 555, 564, 565, 559; 382/232, 244–246; 709/247; 710/68

(56) **References Cited**

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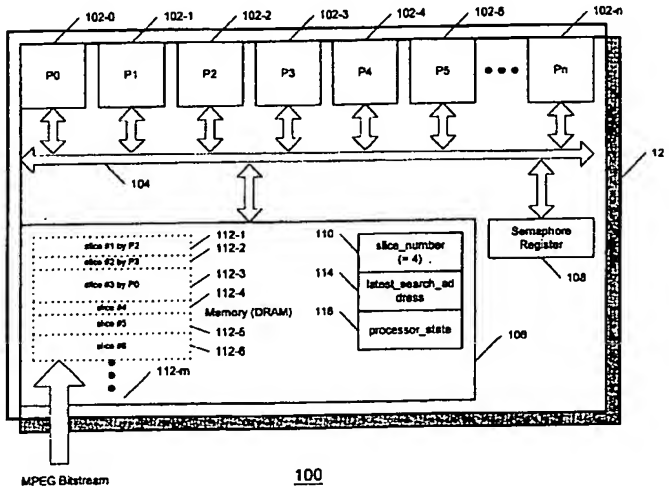
Primary Examiner—Kee M. Tung
(74) *Attorney, Agent, or Firm*—Sawyer Law Group LLP

(57) **ABSTRACT**

A method and system for concurrent processing of slices of a bitstream in a multiprocessor (MP) system is disclosed. The MP system includes a number of identical processors and a common memory. The memory is for receiving a plurality of bitstreams (preferably MPEG2 bitstreams) as a plurality of slices. The method and system comprises accessing a semaphore register by one of the plurality of processors and searching for an associated slice within the memory by the one processor. The method and system further comprises processing the associated slice by the one processor. Finally, the method and system comprises updating a memory location which holds the last address of the associated slice by the one processor; wherein subsequent processors search for each of the plurality of slices from the updated last address in the register. A system and method in accordance with the present invention provides for intercommunication between the plurality of processors within a multiprocessing system. By determining within a semaphore the most recent location of the decoding task, the time and effort spent on searching for new starting location of new task is minimized. Accordingly, the decoding process is parallel, and in most cases averages out the decoding demand on the processors. Accordingly, each of the processors within the multiprocessor system, only needs to search from the address of the bitstream through the remainder of the bitstream to obtain the slice. This process is repeated for each of the processors until the bitstream is processed. Therefore, in a system and method in accordance with the present invention there is no requirement that a processor search from the beginning of the bitstream to the point where the slice originates because the address pointers are updated as at the point where the last slice has been operated on. This provides for a more efficient system for processing bitstreams in a parallel fashion.

14 Claims, 6 Drawing Sheets



General Structure of the Multi-processor System for Efficient MPEG Bitstream Decoding

US006473086B1

(12) **United States Patent**
Morein et al.

(10) **Patent No.: US 6,473,086 B1**
(45) **Date of Patent: Oct. 29, 2002**

(54) **METHOD AND APPARATUS FOR GRAPHICS PROCESSING USING PARALLEL GRAPHICS PROCESSORS**

(75) Inventors: **Stephen L. Morein**, Cambridge, MA (US); **Andrew E. Gruber**, Arlington, MA (US)

(73) Assignee: **ATI International Srl**, Barbados (KN)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/457,649**

(22) Filed: **Dec. 9, 1999**

(51) **Int. Cl.**[7] **G06F 15/80**
(52) **U.S. Cl.** **345/505**; 345/422; 345/537; 345/549; 710/22
(58) **Field of Search** 345/502–506, 345/552, 422, 536–538, 549, 520, 519, 531, 589, 591–593; 710/22, 30, 33

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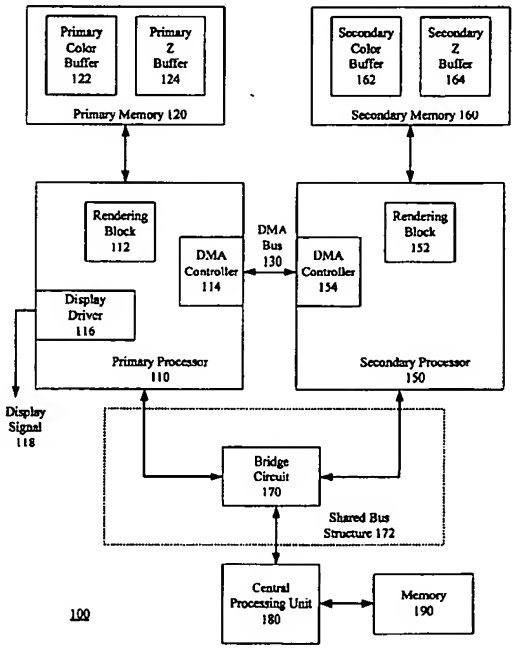
Primary Examiner—Kee M. Tung
(74) *Attorney, Agent, or Firm*—Vedder, Price, Kaufman & Kammholz

(57) **ABSTRACT**

A method and apparatus for graphics processing that utilizes multiple graphics processors in parallel is presented. A primary graphics processor is operably coupled to a primary memory that includes a primary color buffer and a primary Z buffer. The primary processor processes a first portion of the image data for a frame, where processing the first portion stores color data in the primary color buffer and Z data in the primary Z buffer. A secondary processor is operably coupled to a secondary memory that includes a secondary color buffer and a secondary Z buffer. The secondary processor processes a second portion of the image data for the frame. The processing of the second portion of the image data results in color data being stored in the secondary color buffer and Z data being stored in the secondary Z buffer. The display signal that results in the image data for the frame being displayed is generated by a display driver included in the primary processor. In one embodiment, the display driver retrieves all of the color data used to generate the display signal from the primary color buffer. As such, the secondary processor transfers the color data for the second portion of the frame from the secondary color buffer to the primary color buffer to facilitate generation of the display signal. This data transference preferably occurs utilizing direct memory access (DMA) transfers that may be initiated during the vertical blanking interval portion of the display signal.

24 Claims, 4 Drawing Sheets



US006404439B1

(12) **United States Patent**
Coulombe et al.

(10) **Patent No.: US 6,404,439 B1**
(45) **Date of Patent: *Jun. 11, 2002**

(54) **SIMD CONTROL PARALLEL PROCESSOR WITH SIMPLIFIED CONFIGURATION**

(75) Inventors: **Jonathan Coulombe**, Tokyo; **Seiichiro Iwase**, Kanagawa, both of (JP)

(73) Assignee: **Sony Corporation**, Tokyo (JP)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/034,856**

(22) Filed: **Mar. 4, 1998**

(30) **Foreign Application Priority Data**

Mar. 11, 1997 (JP) 9-056232

(51) **Int. Cl.**[7] **G06F 15/80**

(52) **U.S. Cl.** **345/505**; 345/502; 345/503; 345/506; 712/14; 712/20; 712/21; 712/22

(58) **Field of Search** 712/22, 21, 20, 712/14; 345/502, 505, 503, 506; 708/500, 521

(56) **References Cited**

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Primary Examiner—Mark Zimmerman
Assistant Examiner—Kimbinh T. Nguyen
(74) *Attorney, Agent, or Firm*—Frommer Lawrence & Haug LLP; William S. Frommer; Glenn F. Savit

(57) **ABSTRACT**

According to the SIMD control parallel processing method for performing common operation in parallel in a plurality of elements, comprising first retaining means for retaining operation data specified by n-bit for each of said plurality of elements; second retaining means for previously retaining operated result with all possible combinations comprising said data according to a predetermined operation; and selecting means for selecting said operated data retained in said first retaining means from among said operated results retained by said second retaining means, from among retained data obtained through operation, data corresponding to that resultant from the operation is selected for each element, thereby enabling a configuration to be simplified, smaller and less costly.

26 Claims, 20 Drawing Sheets